# Design-for-Adaptivity of Microarchitectures

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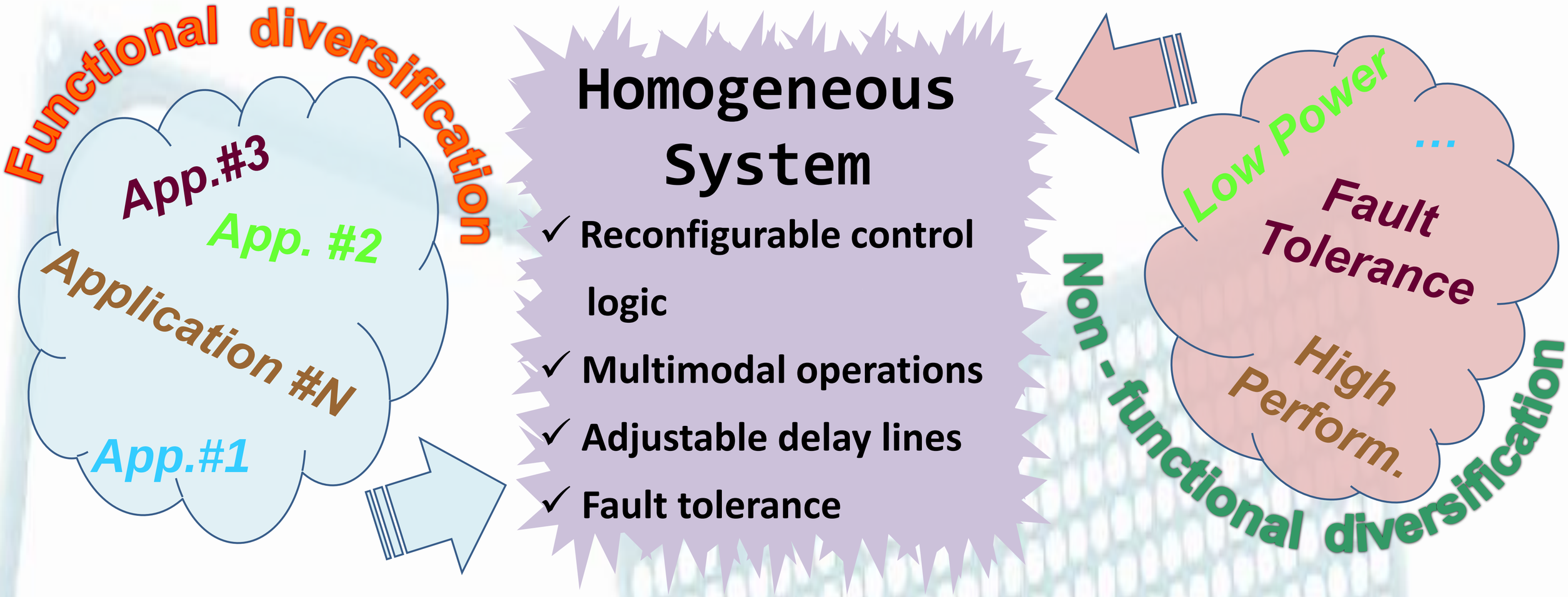
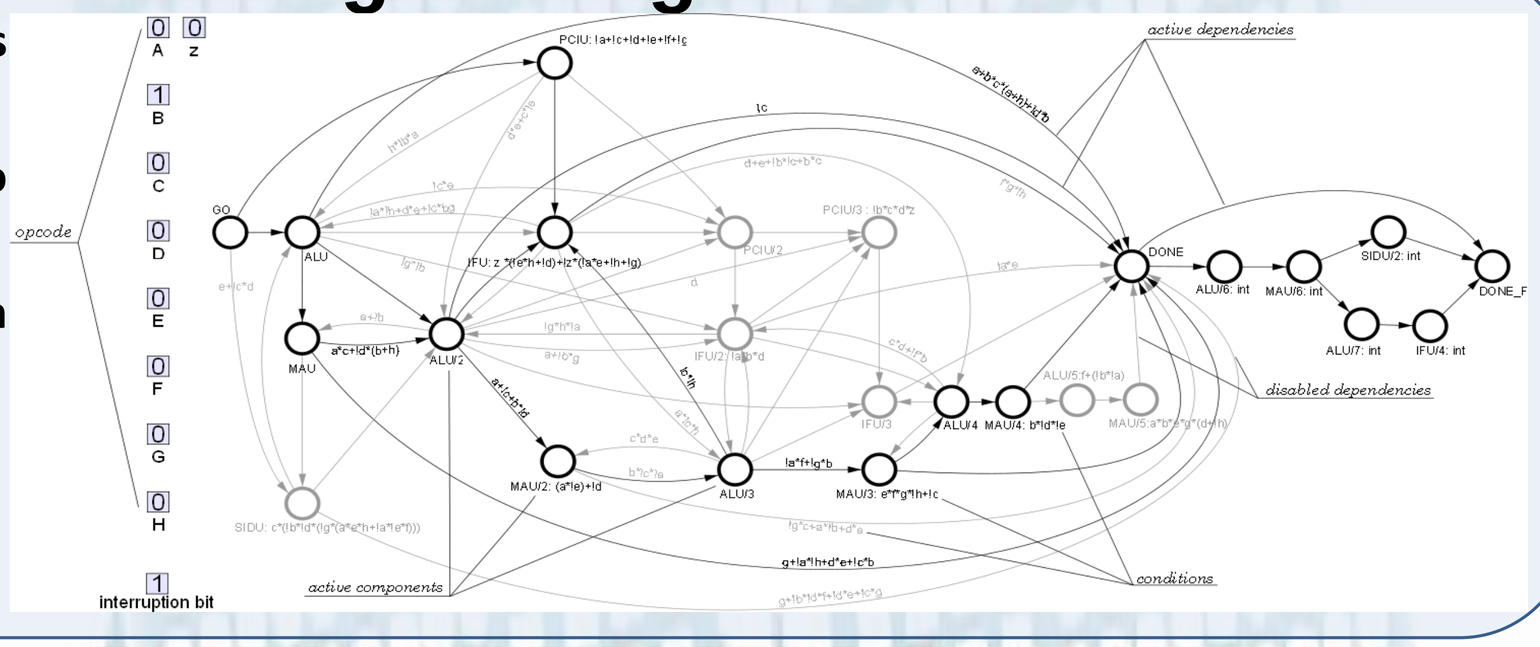


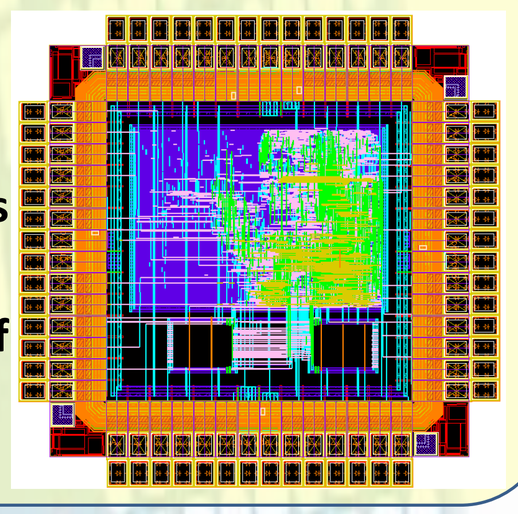

## Novel approach for control logic design

- Capturing common behavioural patterns shared by microprocessor instructions.
- Very compact and efficient way to represent all 257 CPU instructions.
- Easy to reshape for needed instruction set or operating mode.
- Synthesis results:
  - * Top-level control - 326 gates
  - * ALU control - 220 gates



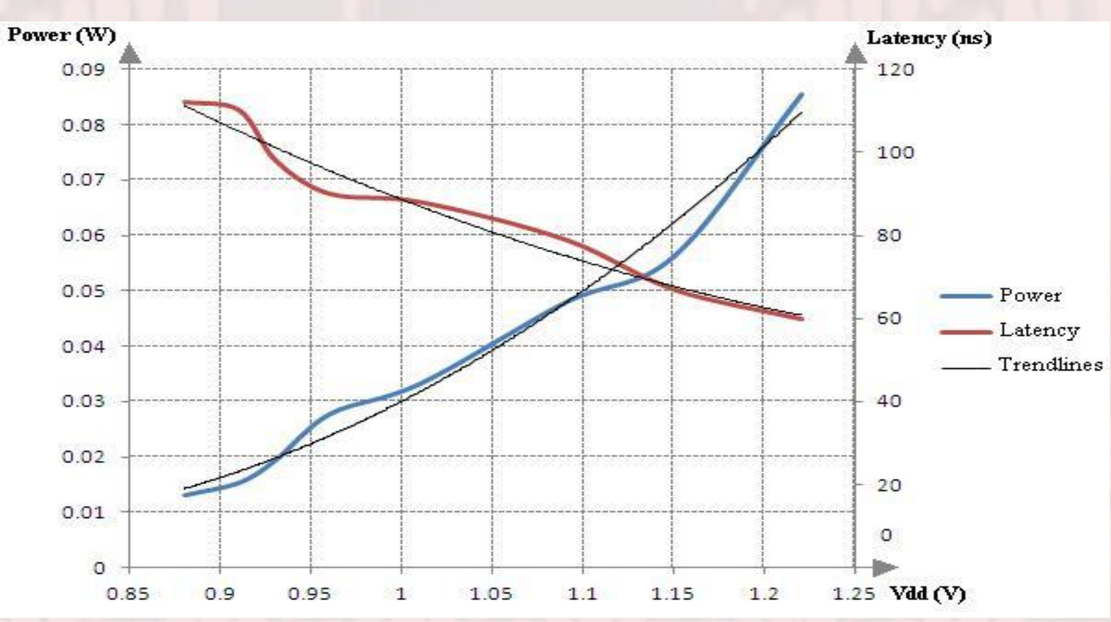

## Asynchronous Intel 8051 implementation

- ASIC implementation of Asynchronous Intel 8051 microprocessor in 130nm technology [1].
- External 128 kB ROM, two internal 4 kB RAM access and interrupt support.
- Extended microprocessor datapath is based on bundled-data approach, which enables multimodal functionality and fault tolerance.
- Adjustable delay lines are used to signal completion of computation in a wide range of operating conditions.
- The total delay latency is formed as a configurable combination of delay segments.



## Achieved Results

| Microprocessor | Technology | MIPS | Average Power, mW | MIPS/W | Energy per instr., pJ |
|---|---|---|---|---|---|
| S80C51 | 3.3V,350nm | 4 | 40 | 100 | 10000 |
| A80C51 | 3.3V,350nm | 4 | 9 | 44 | 2250 |
| H8051 | 3.3V,350nm | 4 | 44.7 | 89.5 | 11175 |
| DS89C420 | 1.1V,350nm | 11 | 18.52 | 600 | 1684 |
| Lutonium | 1.1V,180nm | 100 | 20.7 | 4830 | 207 |
| Nanyang_8051 | 1.1V,350nm | 0.6 | 0.07 | 8000 | 130 |
| **Proposed 8051** | **1.2V,130nm** | **1.5** | **0.74** | **2027** | **493** |




[1] Mokhov A., Rykunov M., Iliasov A., Sokolov D., Yakovlev A., and Romanovsky A. Synthesis of processor instruction sets from high-level ISA specifications. In IEEE Transactions on Computers, 2013.